AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Previously Presented) A memory storage system that is accessed by a first central processing unit (CPU), comprising:

a line cache including a plurality of pages that are accessed by the first CPU;

a first memory device that stores data that is loaded into said line cache when a miss occurs,

wherein when said miss occurs and before a second miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one;

a second memory device; and

a line cache control system that controls data flow between said line cache, the first CPU, said first memory device and said second memory device, and that includes:

a first line cache interface that is associated with the first CPU, that receives a first program read request from the first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with said first memory device;

a second memory interface that communicates with said second memory device; and

a switch that selectively connects said line cache to one of said first and second memory interfaces, wherein when said line cache receives said first address, said line cache control system compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and loads said n pages of said line cache when said miss occurs.

2. (Original) The memory storage system of claim 1 wherein when the first CPU requests data from an m^{th} page of said n pages in said line cache, wherein m is greater than one and less than or equal to n, said line cache loads p additional pages with data from sequential locations in said first memory device.

3. (Cancelled).

4. (Previously Presented) The memory storage system of claim 1 further comprising:

a second CPU;

a second line cache interface that is associated with said second CPU, that receives a second program read request from said second CPU and that generates a second address from said second program read request; and

a line cache arbitration device that communicates with said first and second line cache interfaces and said line cache and that resolves line cache access conflicts between the first CPU and said second CPU.

5. (Previously Presented) A memory storage system that is accessed by a first central processing unit (CPU), comprising:

a line cache including a plurality of pages that are accessed by the first CPU;

a first memory device that stores data that is loaded into said line cache when a miss occurs,

wherein after an initial miss, said line cache prevents any additional misses as long as the first CPU addresses sequential memory locations of said first memory device;

a second memory device; and

a line cache control system that controls data flow between said line cache, the first CPU, said first memory device and said second memory device, and that includes:

a first line cache interface that is associated with the first CPU, that receives a first program read request from the first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with said first memory device;

a second memory interface that communicates with said second memory device; and

a switch that selectively connects said line cache to one of said first and second memory interfaces, wherein when said line cache receives said first address, said line cache control system compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and loads said n pages of said line cache when said miss occurs.

6. (Original) The memory storage system of claim 5 wherein when said miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one.

7. (Original) The memory storage system of claim 6 wherein when the first CPU requests data from an m^{th} page of said n pages in said line cache, wherein m is greater than one and less than or equal to n, said line cache loads p additional pages with data from sequential locations in said first memory device.

8. (Cancelled).

9. (Previously Presented) The memory storage system of claim 5 further comprising:

a second CPU;

a second line cache interface that is associated with said second CPU, that receives a second program read request from said second CPU and that generates a second address from said second program read request; and

a line cache arbitration device that communicates with said first and second line cache interfaces and said line cache and that resolves line cache access conflicts between the first CPU and said second CPU.

10. (Previously Presented) A memory storage system, comprising:

a line cache including a plurality of pages;

a first central processing unit (CPU) that accesses data stored in said line cache;

a first memory device that stores data that is loaded into said line cache when a miss occurs,

wherein when said miss occurs and before a second miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one, and wherein when said first CPU requests data from an m^{th} page of said n pages in said line cache, wherein m is greater than one and less than or equal to n, said line cache loads p additional pages with data from sequential locations in said first memory device;

a second memory device; and

a line cache control system that controls data flow between said line cache, said first CPU, said first memory device and said second memory device, and that includes:

a first line cache interface that is associated with said first CPU, that receives a first program read request from said first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with said first memory device;

a second memory interface that communicates with said second memory device; and

a switch that selectively connects said line cache to one of said first and second memory interfaces, wherein when said line cache receives said first address, said line cache control system compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and retrieves said n pages of line cache when said miss occurs.

11. (Cancelled).

12. (Previously Presented) The memory storage system of claim 10 further comprising:

a second CPU;

a second line cache interface that is associated with said second CPU, that receives a second program read request from said second CPU and that generates a second address from said second program read request; and

a line cache arbitration device that communicates with said first and second line cache interfaces and said line cache and that resolves line cache access conflicts between said first CPU and said second CPU.

13. (Previously Presented) A memory storage system, comprising:

a line cache including a plurality of pages;

a first central processing unit (CPU) that accesses said pages of said line cache;

a first memory device that stores data that is loaded into said line cache when a miss occurs,

wherein after an initial miss, said line cache prevents any additional misses as long as said first CPU addresses sequential memory locations of said first memory device;

a second memory device; and

a line cache control system that controls data flow between said line cache, said first CPU, said first memory device and said second memory device, and that includes:

a first line cache interface that is associated with said first CPU, that receives a first program read request from said first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with said first memory device;

a second memory interface that communicates with said second memory device; and

a switch that selectively connects said line cache to one of said first and second memory interfaces, wherein when said line cache receives said first address, said line cache control system compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and loads said n pages of said line cache when said miss occurs.

14. (Original) The memory storage system of claim 13 wherein when said miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one.

15. (Original) The memory storage system of claim 14 wherein when said first CPU requests data from an m^{th} page of said n pages in said line cache, wherein m is greater than one and less than or equal to n, said line cache loads p additional pages with data from sequential locations in said first memory device.

16. (Cancelled).

17. (Previously Presented) The memory storage system of claim 13 further comprising:

a second CPU;

a second line cache interface that is associated with said second CPU, that receives a second program read request from said second CPU and that generates a second address from said second program read request; and

a line cache arbitration device that communicates with said first and second line cache interfaces and said line cache and that resolves line cache access conflicts between said first CPU and said second CPU.

18. (Currently Amended) A storage system comprising:

a first memory interface;

a second memory interface;

a first memory that communicates exclusively with said first memory interface;

a second memory that communicates exclusively with said second memory interface;

a cache that stores data from said first and second memories and receives a data request from a processor specifying a first address, wherein when requested data corresponding to said first address is present in said cache, said cache provides said requested data to the processor; and

a switch that communicates with said cache, wherein when said requested data is not present in said cache, said switch exclusively connects one of said first memory interface and said second memory interface to said cache, as selected by said first address, whereby said cache retrieves said requested data,

wherein after a first time that said requested data is not present in said cache, n pages of said cache are loaded with data from sequential locations of one of said first and second ~~memory devices~~ memories to prevent any additional cache misses for as long as sequential memory locations of said one of said first and second ~~memory devices~~ memories are addressed.

19. (Previously Presented) The storage system of claim 18 wherein said cache translates an address contained within said data request to obtain said first address.

20. (Previously Presented) The storage system of claim 18 wherein said first memory interface also communicates with the processor via a first direct interface, which bypasses the cache for selected accesses to said first memory.

21. (Previously Presented) The storage system of claim 20 wherein when said first address is located within said first memory, writes to said first address can only be performed via said first direct interface.

22. (Previously Presented) The storage system of claim 21 wherein said first memory comprises flash memory, said first direct interface is used to program said first memory, and said cache retrieves data from said first memory interface as a burst.

23. (Previously Presented) The storage system of claim 20 wherein said second memory interface also communicates with the processor via a second direct interface, which bypasses the cache for selected accesses to said second memory.

24. (Previously Presented) The storage system of claim 23 wherein when said first address is located within said second memory, writes to said first address can only be performed via said second direct interface.

25. (Previously Presented) The storage system of claim 18 wherein said cache is comprised of a plurality of lines, and when said requested data is not present in said cache, said cache fills one line with data including said requested data and fills at least one more line with data adjacent to said requested data.

26. (Currently Amended) A storage system comprising:

a first memory interface;

a second memory interface;

a first memory that communicates exclusively with said first memory interface;

a second memory that communicates exclusively with said second memory interface;

an arbitration module that receives data requests from first and second processors, and processes said data requests into ordered data requests;

a cache that stores data from said first and second memories and receives one of said ordered data requests specifying a first address and associated with one processor of the first and second processors, wherein when requested data corresponding to said first address is present in said cache, said cache provides said requested data to the one processor; and

a switch that communicates with said cache, wherein when said requested data is not present in said cache, said switch exclusively connects one of said first memory interface and said second memory interface to said cache, as selected by said first address, whereby said cache retrieves said requested data,

wherein after a first time that said requested data is not present in said cache, n pages of said cache are loaded with data from sequential locations of one of said first and second ~~memory devices~~ memories to prevent any additional cache misses for as long as sequential memory locations of said one of said first and second ~~memory devices~~ memories are addressed.

27. (Previously Presented) The storage system of claim 26 wherein said cache translates an address contained within said ordered data request to obtain said first address.

28. (Previously Presented) The storage system of claim 26 wherein said first memory interface also communicates with the second processor via a direct interface, which bypasses the cache for selected accesses to said first memory.

29. (Previously Presented) The storage system of claim 28 wherein when said first address is located within said first memory, writes to said first address can only be performed via said direct interface.

30. (Currently Amended) The storage system of claim 29 wherein said first memory comprises flash memory, said ~~first~~ direct interface is used to program said first memory, and said cache retrieves data from said first memory interface as a burst.

31. (Previously Presented) The storage system of claim 28 wherein said second memory interface also communicates with the first and second processors via a direct arbitration interface, which bypasses the cache for selected accesses to said second memory.

32. (Currently Amended) The storage system of claim 31 wherein when said first address is located within said second memory, writes to said first address can only be performed via said ~~second~~ direct arbitration interface.

33. (Previously Presented) The storage system of claim 26 wherein said cache is comprised of a plurality of lines, and when said requested data is not present in said cache, said cache fills one line with data including said requested data and fills at least one more line with data adjacent to said requested data.